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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,205	01/20/2004	Akira Hokazono	247866US2S	7742
22850	7590	06/29/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			MAGEE, THOMAS J	
			ART UNIT	PAPER NUMBER
			2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

AL

Office Action Summary	Application No. 10/759,205	Applicant(s) HOKAZONO ET AL.	
	Examiner Thomas J. Magee	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>01202004</u> | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Claim Rejections – 35 U.S.C. 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 – 4, 6 – 9, 11 – 13, and 15 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al. (US 6,235,568 B1) in view of Stevens et al. (US 5,170,242)

3. Regarding Claims 1 and 2, Murthy et al. disclose a semiconductor device comprising:

a p-type silicon semiconductor region (202) (Figure 2f) (Col. 4, line 13 – 14),

an n-type diffusion region (224) formed in a surface region of the silicon semiconductor region, and

a Ni silicide film (240) (Figure 2k) formed in a surface region of the n-type diffusion region.

Murthy et al. do not disclose that a p-type impurity diffusion layer formed to extend from a surface of the Ni silicide film in a depth direction. Stevens et al. disclose the presence of a Ni silicide layer (Col. 5, lines 30 – 32) into which a p-type impurity (boron) is implanted such that the impurity profile has a peak concentration within the silicide film (Col. 5, lines 42 – 43). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Stevens et al. and Murthy et al. to obtain a barrier to prevent loss of impurities in underlying material from diffusing to grain boundaries of the silicide (Stevens et al., Col. 1, lines 38 – 44).

Additionally, Murthy et al. do not disclose that the diffusion layer has a peak concentration not lower than $1E20/cm^3$ at a preset depth and a concentration beyond an interface not higher than $5E19/cm^3$. However, it is routine in the art to conduct a series of tests to optimize doping profiles in doped layers and it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize parameters to attain the doping profile as claimed in order to form an impurity doped contact region that would improve interface adhesion and grain boundary blocking for a device of improved reliability.

4. Regarding Claims 3, 8, 13, and 17, Murthy et al. do not disclose that the peak concentration occurs at a depth of 30 nm from the surface of the film. Stevens et al. disclose that the p-type impurity (boron) profile has a peak concentration at a depth of 0.03 μm (30 nm) from the surface of the Ni silicide film (Col. 5, lines 30 – 32). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Stevens et al. and Murthy et al. to obtain a barrier to prevent loss of impurities in underlying material from diffusing to grain boundaries of the silicide (Stevens et al., Col. 1, lines 38 – 44).

5. Regarding Claims 4 and 9, Murthy et al. disclose a semiconductor device wherein the n-type diffusion region is a source/drain region of the transistor (224) (Col. 6, lines 23 – 28).

6. Regarding Claim 6, Murthy et al. disclose a semiconductor device comprising:

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a p-type silicon semiconductor region (202) (Figure 2f) (Col. 4, line 13 – 14),

a pair of n-type diffusion regions (224) separately formed in a surface region of the silicon semiconductor region,

a gate electrode (206) (Col. 4, lines 49 – 53) containing silicon and formed above part of the semiconductor region which lies between n-diffusion regions with a gate insulating film (203) (Col. 4, line 49) interposed therebetween,

a plurality of Ni silicide films (240) (Figure 2I) formed in surface regions of the pair of n-type diffusion regions (224) and in the upper surface region of the gate electrode.

Murthy et al. do not disclose that a p-type impurity diffusion layer formed to extend from a surface of the Ni silicide film in a depth direction. Stevens et al. disclose the presence of a Ni silicide layer (Col. 5, lines 30 – 32) into which a p-type impurity (boron) is implanted such that the impurity profile has a peak concentration within the silicide film (Col. 5, lines 42 – 43). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Stevens et al. and Murthy et al. to obtain a barrier to prevent loss of impurities in underlying material from diffusing to grain boundaries of the silicide (Stevens et al., Col. 1, lines 38 – 44).

Additionally, Murthy et al. do not disclose that the diffusion layer has a peak concentration not lower than $1E20/cm^3$ at a preset depth and a concentration beyond an interface not higher than $5E19/cm^3$. However, it is routine in the art to conduct a series of tests to optimize doping profiles in doped layers and it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize parameters to attain the doping profile as claimed in order to form an impurity doped contact region that would improve interface adhesion and grain

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boundary blocking for a device of improved reliability.

7. Regarding Claims 11, 12, 15, and 16, Murthy et al. disclose a manufacturing method of a semiconductor device comprising:

doping n-type ions (224) (Col. 6, line 59) into a selected portion of a surface region of a p-type silicon semiconductor region (202) (Col. 4, line 13),

doping p-type impurity ions (234) (Figure 2h) into the entire surface region of the silicon semiconductor region (Col. 7, lines 5 –9),

activating n-type (source/drain) and p-type (tip implants) impurity ions to form an n-type diffusion region (224) in the surface region and a p-type impurity diffusion layer in a depth direction, and

performing a heat treatment to form a Ni silicide film in the surface region of the n-type diffusion region (Col. 9, lines 26 – 30) after depositing Ni (Col.9, lines 22 – 26) on the surface of the n-type diffusion region.

Murthy et al. do not disclose that a p-type impurity diffusion layer formed to extend from a surface of the Ni silicide film in a depth direction. Stevens et al. disclose the presence of a Ni silicide layer (Col. 5, lines 30 – 32) into which a p-type impurity (boron) is implanted such that the impurity profile has a peak concentration within the silicide film (Col. 5, lines 42 – 43). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Stevens et al. and Murthy et al. to obtain a barrier to prevent loss of impurities in underlying material from diffusing to grain boundaries of the silicide (Stevens et al., Col. 1, lines 38 – 44).

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Additionally, Murthy et al. do not disclose that the diffusion layer has a peak concentration not lower than $1E20/cm^3$ at a preset depth and a concentration beyond an interface not higher than $5E19/cm^3$. However, it is routine in the art to conduct a series of tests to optimize doping profiles in doped layers and it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize parameters to attain the doping profile as claimed in order to form an impurity doped contact region that would improve interface adhesion and grain boundary blocking for a device of improved reliability.

8. Claims 5, 10, 14, and 18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al. in view of Stevens et al., as applied to Claims 1 – 4, 6 – 9, 11 – 13, and 15 – 17, and further in view of Tanaka et al. (US 6,790,723 B2).

9. Regarding Claim 5, Murthy et al. do not disclose a contact liner film formed on the n-type diffusion region with an opening portion to expose part of the surface of the n-type diffusion region and an electrode in contact with the surface of the region. Tanaka et al. disclose the presence of a contact liner film (415) (Figure 30A) formed on the n-type diffusion region (413) with an opening portion to expose the surface and an electrode (407) formed in contact with the surface. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Tanaka et al. with Murthy et al. to obtain contact structure for a more efficient working device.

10. Regarding Claim 10, as discussed above, Murthy et al. do not disclose the presence of liner

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films on n-type diffusion regions with openings over the regions and electrodes formed in contact with the surface. Tanaka et al. disclose a liner film (415) on at least a pair of n-diffusion regions (since the structure in Figure 30A is repetitive) with corresponding openings and electrodes (407) formed in the openings. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Tanaka et al. with Murthy et al. to obtain contact structure for a more efficient working device.

11. Regarding Claims 14 and 18, Murthy et al. do not disclose a contact liner film formed on the entire surface after formation of the Ni silicide and an inter-level insulating film on the entire surface with an opening portion to expose part of the surface of the n-type diffusion region through the insulating film and liner film, and an electrode in contact with the surface of the region. Tanaka et al. disclose:

forming a contact liner film (415) (Figure 30A) on the entire surface of the device,

forming an inter-level insulating film (406) on the entire surface,

forming an opening portion which reaches the surface of the n-type diffusion region (413) in (through) the insulating film (406) and liner film (415), and

forming an electrode (407) in contact with the surface of the n-type diffusion region (413) in the opening portion.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Tanaka et al. with Murthy et al. to obtain contact structure for a more efficient working device.

12. Claims 19 – 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al. in view of Stevens et al.

13. Regarding Claims 19 and 20, Murthy et al. disclose a manufacturing method of a semiconductor device comprising:

doping n-type ions (224) (Col. 6, line 59) into a selected portion of a surface region of a p-type silicon semiconductor region (202) (Col. 4, line 13),

activating the n-type impurity ions to form an n-type diffusion region on the surface portion of the silicon semiconductor region (Col. 6, lines 47 – 53),

activating the p-type impurity ions (tip implants) to form p-type diffusion region (Col. 6, lines 47 – 53), in a depth direction of the semiconductor region, and

performing a heat treatment to form a Ni silicide film in the surface region of the n-type diffusion region (Col. 9, lines 26 – 30) after depositing Ni (Col.9, lines 22 – 26) on the surface of the n-type diffusion region.

Murthy et al. do not disclose that a p-type impurity diffusion layer formed to extend from a surface of the Ni silicide film in a depth direction. Stevens et al. disclose the presence of a Ni silicide layer (Col. 5, lines 30 – 32) into which a p-type impurity (boron) is implanted such that the impurity profile has a peak concentration within the silicide film (Col. 5, lines 42 – 43). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Stevens et al. and Murthy et al. to obtain a barrier to prevent loss of impurities in underlying material from diffusing to grain boundaries of the silicide (Stevens et al., Col. 1, lines 38 – 44).

Additionally, Murthy et al. do not disclose that the diffusion layer has a peak concentration not lower than $1 \times 10^{20}/\text{cm}^3$ at a preset depth and a concentration beyond an interface not higher than $5 \times 10^{19}/\text{cm}^3$. However, it is routine in the art to conduct a series of tests to optimize doping profiles in doped layers and it would have been obvious to one of ordinary skill in the art at the time of the invention to optimize parameters to attain the doping profile as claimed in order to form an impurity doped contact region that would improve interface adhesion and grain boundary blocking for a device of improved reliability.

14. Regarding Claim 21, Murthy et al. do not disclose that the peak concentration occurs at a depth of 30 nm from the surface of the film. Stevens et al. disclose that the p-type impurity (boron) profile has a peak concentration at a depth of 0.03 μm (30 nm) from the surface of the Ni silicide film (Col. 5, lines 30 – 32). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Stevens et al. and Murthy et al. to obtain a barrier to prevent loss of impurities in underlying material from diffusing to grain boundaries of the silicide (Stevens et al., Col. 1, lines 38 – 44).

15. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murthy et al. in view of Stevens et al, as applied to Claims 19 – 21, and further in view of Tanaka et al.

16. Regarding Claim 22, Murthy et al. do not disclose a contact liner film formed on the entire surface after formation of the Ni silicide and an inter-level insulating film on the entire surface with an opening portion to expose part of the surface of the n-type diffusion region through the

insulating film and liner film, and an electrode in contact with the surface of the region. Tanaka et al. disclose:

forming a contact liner film (415) (Figure 30A) on the entire surface of the device,
forming an inter-level insulating film (406) on the entire surface,
forming an opening portion which reaches the surface of the n-type diffusion region (413)
in (through) the insulating film (406) and liner film (415), and
forming an electrode (407) in contact with the surface of the n-type diffusion region (413)
in the opening portion.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Tanaka et al. with Murthy et al. to obtain contact structure for a more efficient working device.

Response to Arguments

17. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusions

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658**. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's acting supervisor, **Stephen Loke**, can be reached on **(571) 272-1657**. The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306**.

Thomas Magee
June 22, 2005

Stephen Loke
Primary Examiner